**REPORT**

**Synthesis and Implementation**

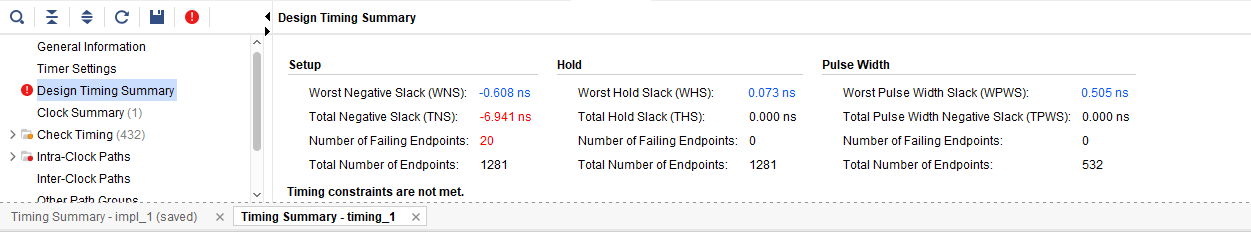
1. **Timing Analysis**

**At 3ns**

Setup Time Violation

* worst negative slack (WNS) is negative, indicating a setup time violation

**create\_clock -add -name sys\_clk\_pin -period 3.00 [get\_ports {clk}];**

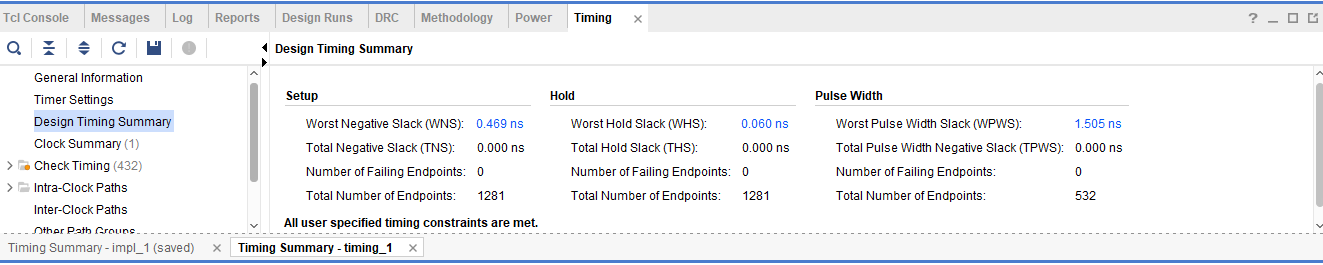


**At 4ns**

Setup Time Violation resolved

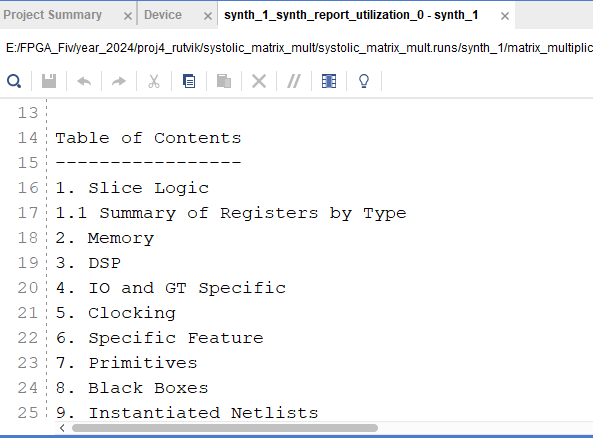
**create\_clock -add -name sys\_clk\_pin -period 4.00 [get\_ports {clk}];**

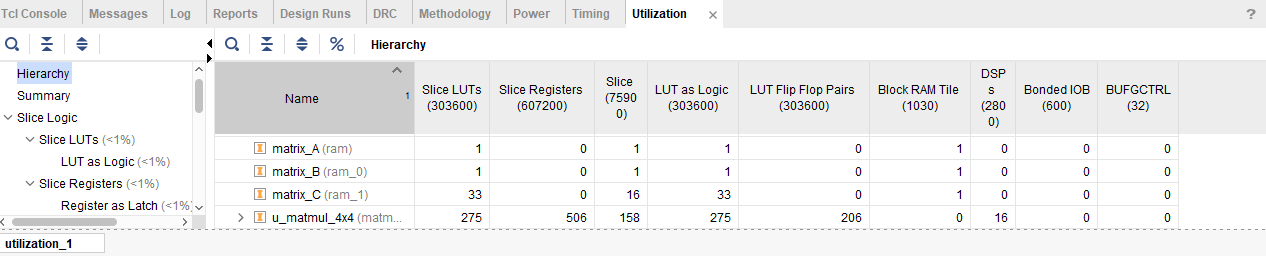
* To fix the above violation, make the WNS positive, this can be done by increasing the clock period.
* Increasing the clock period extends the time available for signals to propagate through the circuit, ensuring that the input signals stabilize sufficiently before being captured by flip-flops, thereby preventing setup time violations. In this scenario, extending the clock period from 3ns to 4ns allows more time for signal propagation and settling, resolving the setup time violation.



1. **Resource Utilization Report**

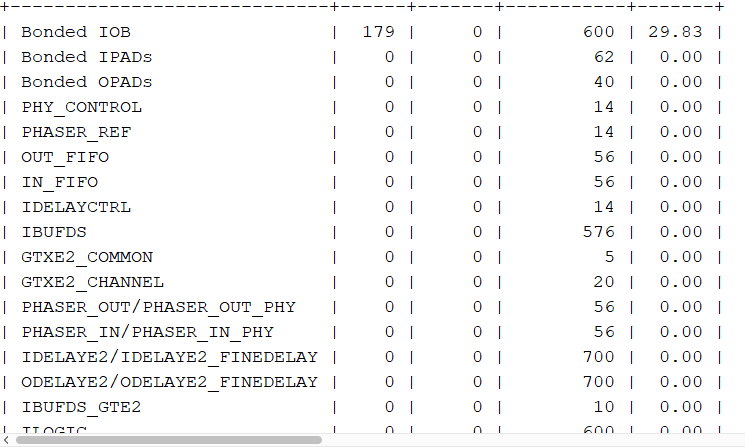
* It is checked, that there’s 16 DSPs and 3 BRAMs being used





1. **Extra Credit (I/O Utilization)**

* Utilzation of I/O is 29.83 %.



**Largest port size temporarily set to 1-bit wide**

* We see that initially it is 29.83% and now it decreases to 19.50%.

